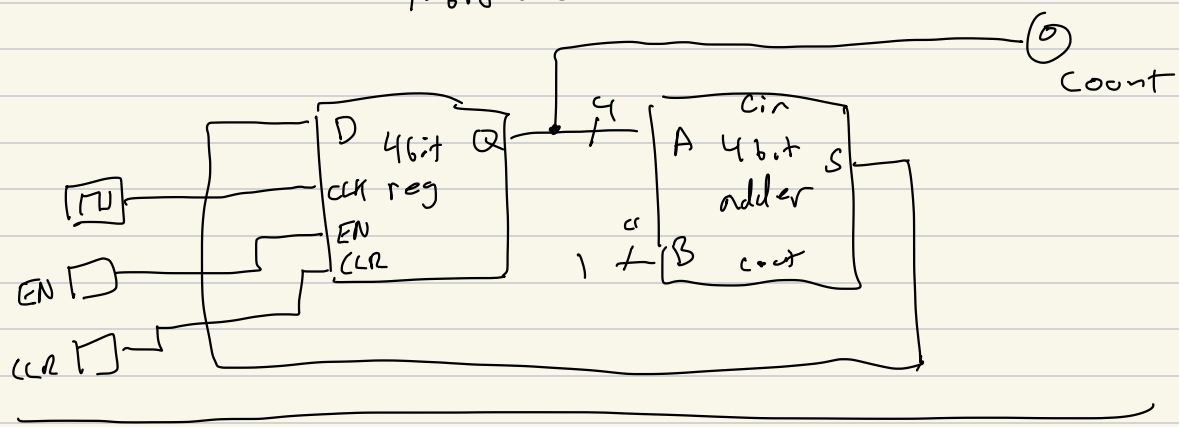
CS 631-02 Processor Design Components

2026-04-09

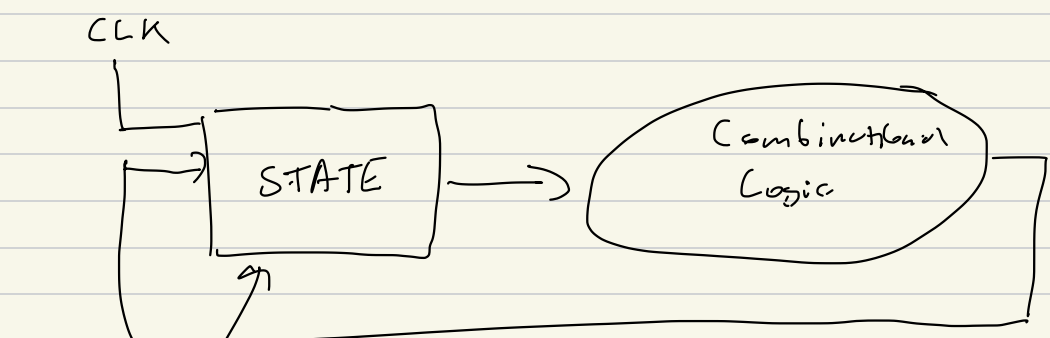
Combinational Logic → gates, sum-of-products

Sequential Logic → latches, D flipflops, register
Clock, multiplexor

Counter 4-bit Counter



Processor



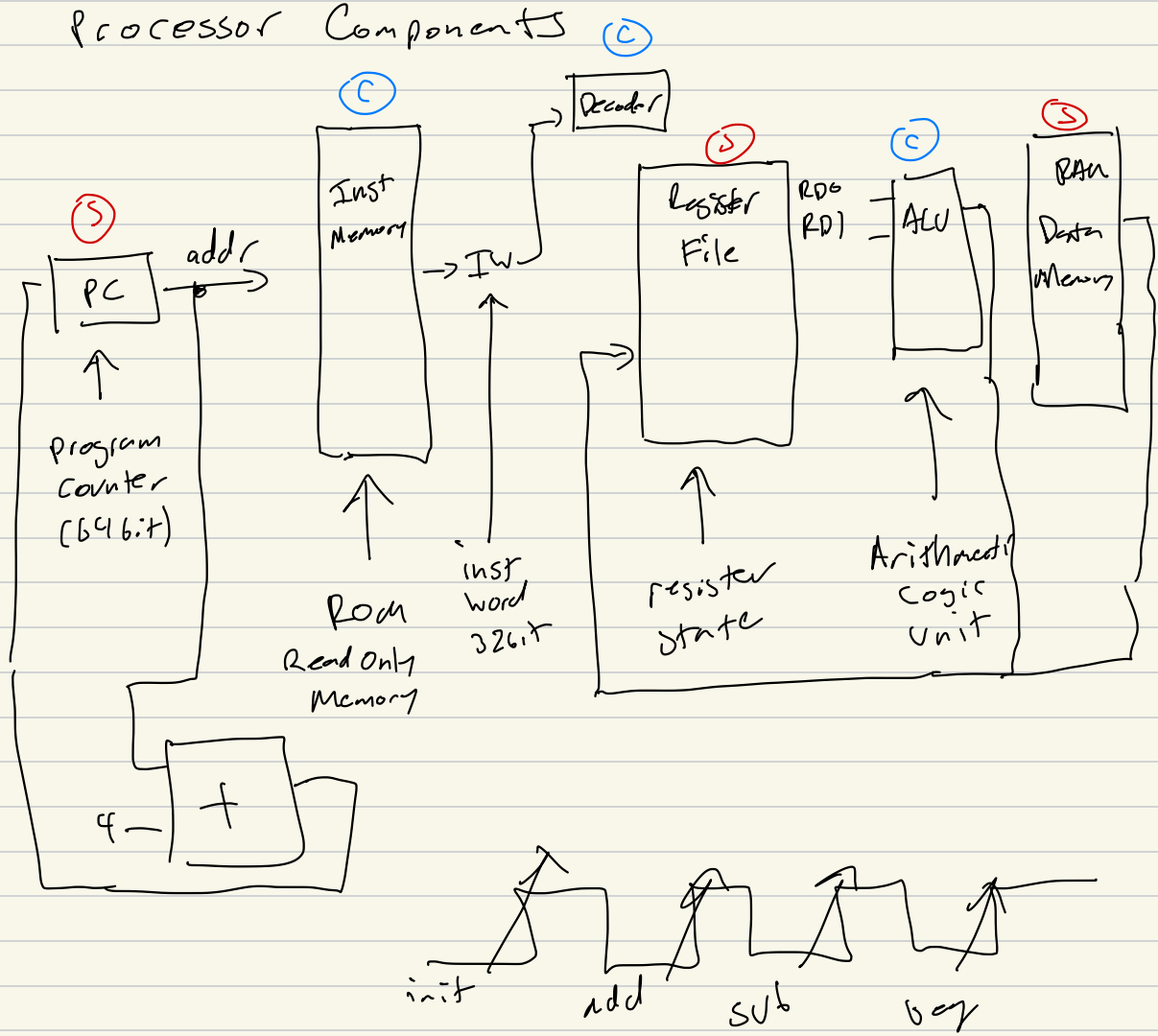
Registers x0-x31 | PC | Data memory

add t0, t1, t2

rd

PC = PC + 4

Processor Components



single-cycle processor

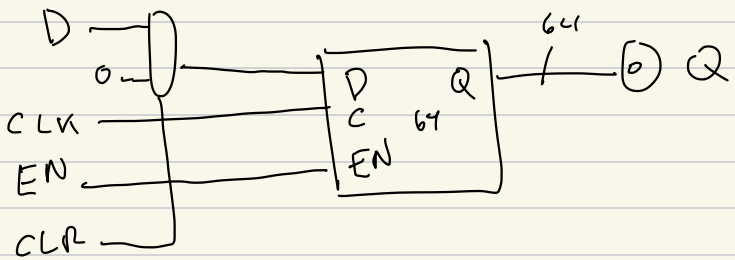
↓

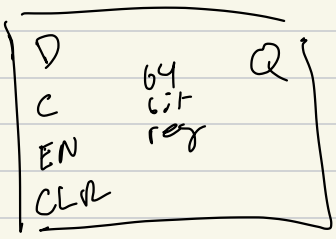
multi-cycle process

↓

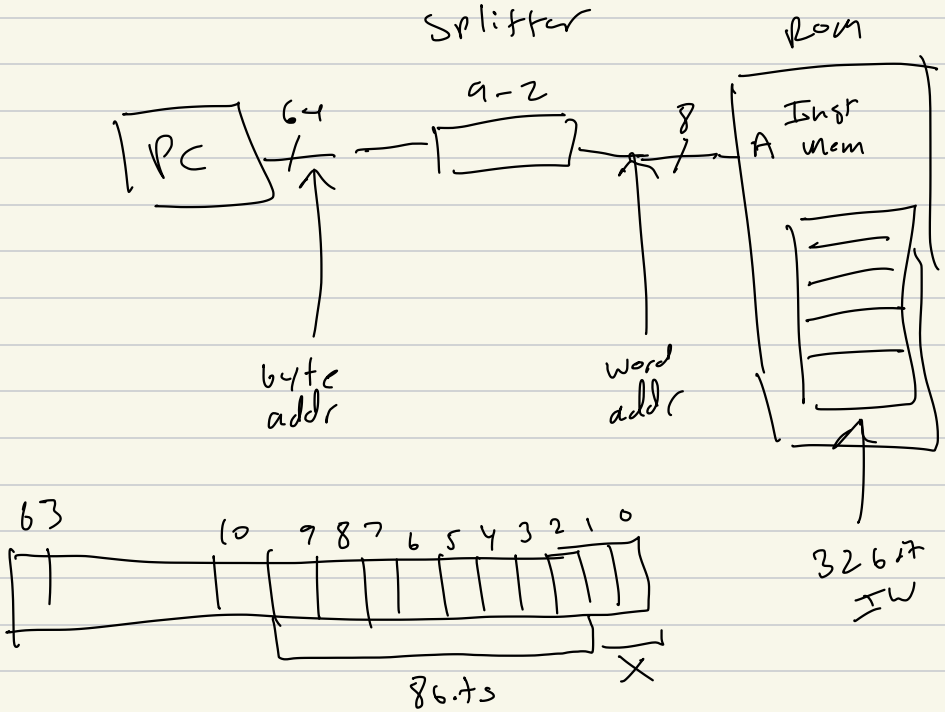
pipelined processor

PC Program Counter

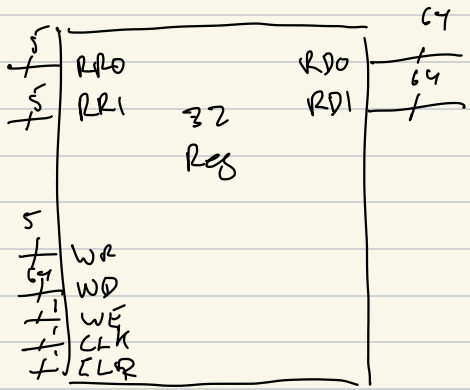




Instruction Memory



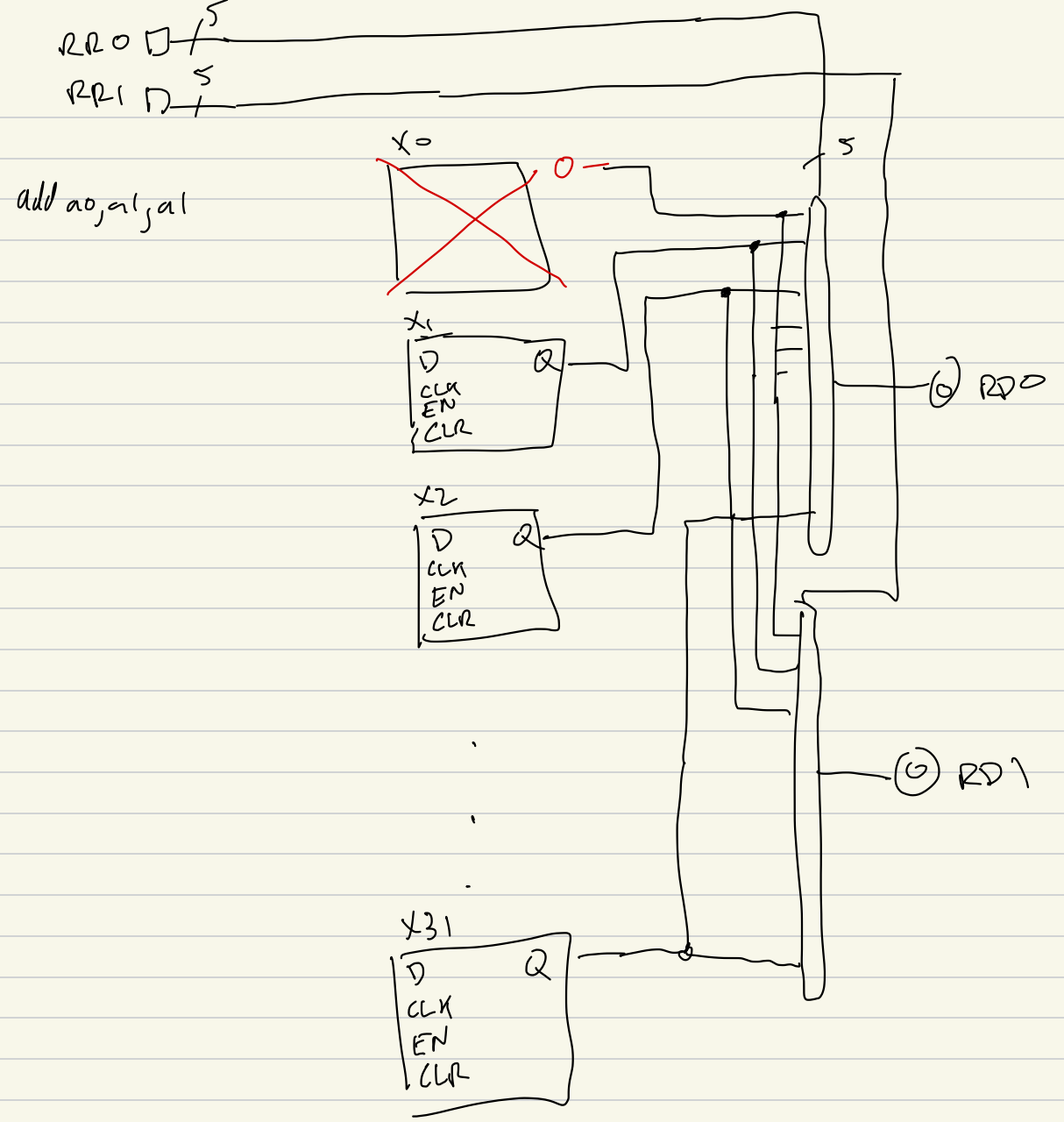
Register File



RR - read reg #
RD - read data value

WR - write reg
WD - write data
WE - write enable

On a single clock cycle
1) read up to two reg values
2) write at most one reg


RR0
5
RR1
5
add a0,a1,a1
X0
0
5
X1
D
Q
CLK
EN
CLR
RD0
X2
D
Q
CLK
EN
CLR
RD1
X31
D
Q
CLK
EN
CLR